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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,276	08/10/2001	Chris Macris		7452

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EXAMINER	
PARSONS, THOMAS H	

ART UNIT	PAPER NUMBER
1745	

DATE MAILED: 03/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

AS-5

Office Action Summary	Application No.	Applicant(s)	
	09/927,276	MACRIS, CHRIS	
	Examiner	Art Unit	
	Thomas H Parsons	1745	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4,13-21 and 35-42* is/are allowed.

6)☒ Claim(s) *5,7-9,12,22,23,25,27,28,30-34,43,46 and 48-52* is/are rejected.

7)☒ Claim(s) *6,10,11,24,26,29,44-45 and 47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 1:

Line 8, suggest changing U.S. Patent Application Serial" to --Application--;

After line 10, suggest inserting the heading "Background of the Invention";

Line 19, suggest changing "Background of the Invention" to --Description of the Related Art--;

Page 4:

Line 38, suggest deleting the first occurrence of "a";

Page 6:

Line 14, suggest changing "is" to --in--;

Page 8:

Line 11, suggest inserting "is" after "invention";

Page 10:

Line 4, suggest inserting "illustrate" before "one";

Line 6, suggest inserting "illustrate" before "another";

Line 35, suggest changing "Best Mode for Carrying Out the Invention" to Detailed Description of the Invention--.

Appropriate correction is required.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. Note also that page 9, lines 30-31 discloses that this figure represents heat flows in a **typical** heat sink. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The Figures 12 through 15 are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: reference sign "30", "32", "96", "98", "100", "102", and "104". A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 5, 9, 12, 22-23, 25, 27-28, 30, and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Burward-Hoy (5,637,921) as further evidenced by Mansuria et al. (5,032,897).

Claim 5: Burward-Hoy discloses in Figures 1 and 2 a heat dissipating IC device comprising one IC die comprising a semiconductor substrate 103 including one circuitry layer (IC chip 101) with a hot region on at least one substrate (i.e. the hot region would be that side of the substrate to which the die is connected); at least one electrically conductive or semiconductive member (201) attachable to the semiconductive substrate; and an electrical source (not shown) connected (via power lines 265 and 270) to the electrically conductive or semiconductive member (201) whereby charge carrier (heat) flow travels in a direction from the hot region (plate 225) on the semiconductor substrate face outward toward the perimeter (flow lines 106) (col. 1: 23-63; and col. 2: 29-col. 3: 54).

Mansuria et al. is cited to show that heat flow would inherently provide charge carrier flow from a hot to a cold region (col. 1:7-40)

Claims 9 and 25: Burward-Hoy discloses in Figure 2 a package (202, 205, 212) for housing an IC die (235) col. 2: 49-col. 3: 54).

Claims 12 and 34: Burward-Hoy discloses in Figure 2 that the semiconductor substrate attachment (23) to the conductive or semiconductive member (201) is conductive (copper block 230).

Claim 22: Burward-Hoy discloses in Figures 1 and 2 a heat dissipating IC device comprising one IC die comprising a semiconductor substrate 103 including one circuitry layer (IC chip 101), the substrate attachable to a heat sink/spreader structure (201, 250, 255)

comprising a heat sink/spreader structure wherein at least one semiconductor is bonded to at least one dissimilar conductor thereby creating a thermoelement couple; and the dissimilar conductor comprises a heat absorbing junction (cold side) and a heat rejecting junction (hot side) (col. 1: 23-63; and col. 2: 29-col. 3: 54).

Claim 23 and 28: Burward-Hoy discloses in Figure 2 a heat absorbing junction positioned near the center of the device and heat rejection junction positioned near the perimeter of the device (In Figure 2 the area of device 201 coupled to IC chip 235 would represent a heat absorbing junction as well as a heat rejection junction because with the application of a current heat is transferred from plate 225 in contact with IC chip 235 to the second plate 225 wherein heat transfer assembly transfers heat away from plate 215; those areas of the device 201 not coupled to the IC chip 235 would represent a heat rejection junction for similar reasons and are shown as located outside a bond line between the semiconductor substrate and the heat sink spreader structure, the bond being line defined by the semiconductor substrate and that area of device 201 contacting the semiconductor substrate).

Claim 27: Burward-Hoy discloses in Figure 2 that the heat sink/spreader structure (201, 250, 255) is larger in overall area that the semiconductor substrate (235).

Claim 30: Burward-Hoy discloses on col. 3:20-39 that a voltage is applied to the thermoelement couple.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7, 8, 31, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burward-Hoy as applied to claim 1 above, and further in view of Bhatia (6,094,919).

Burward-Hoy is as applied, argued and disclosed above, and incorporated herein.

Claims 7 and 31: Burward-Hoy does not disclose that the electrically conductive member is electrically in series with an electrical load other than itself. Bhatia in Figure 2 discloses that the electrically conductive member (35) is electrically in series with an electrical load (circuit board 40) col. 3: 47-58).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the apparatus of Burward-Hoy by incorporating the electrical load of Bhatia because Bhatia teaches that it would have been known to apply an electrically conductive member electrically in series with an electrical load to provide for operating the IC at significantly reduced temperatures thereby resulting in lower cost and more efficient heat dissipation, especially at the system level.

Claims 8 and 32: The recitation "utilized as a resistive load for an electric component" has been construed as a process limitation which does not alter the overall physical structure of the claimed device and is, therefore, given little patentable weight. However, because the device of the Burward-Hoy combination is structurally the same as that instantly claimed, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the device of the Burward-Hoy combination would provide the claimed utility.

Claim 33: As to the recitation "voltage and current is generated...and is consumed by an external electric load", the rejection is as set forth above in claims 8 and 31.

8. Claim 43, 46, 48, and 50-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burward-Hoy (5,637,921), and further in view of Buist (5,022,928).

Claim 43: Burward-Hoy discloses Figures 1-3 a heat dissipating IC device including one IC die comprising a semiconductor substrate (103) including one circuitry layer (IC chip 101) on at least one substrate, more than one thermoelement couple stage (301), each stage containing at least one thermoelement couple, each with at least one heat absorbing (cold side) and heat rejection junction (hot side)(col. 1: 23-63; and col. 2: 29-col. 3: 54).

Burward-Hoy does not disclose all thermoelements fabricated within at least one semiconductor substrate.

Buist discloses in Figure 2d more that one thermoelement couple stage wherein all thermoelements are fabricated within at least one semiconductor substrate (col. 2:56-col. 4: 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device of Burward-Hoy by substituting the thermocouple stage with the thermocouple stage of Buist because Buist teaches a thermoelement couple stage that would have provided a thermoelectric heat pump or power source device that is flexible, planar, economical to fabricate, and of a size small enough for use in connection with all applications presently available in the market place thereby providing cost advantages and a device of high utility.

Claim 46: Burward-Hoy discloses in Figure 2a, 2c and 2d heat absorbing junctions (cold core 28) positioned near the center of each thermoelement couple stage and heat rejection junctions (hot annular ring) positioned near the perimeter of each stage (col. 2:56-col. 4: 2).

Claim 48: Burward-Hoy discloses on col. 3:20-39 that a voltage is applied (via leads 265, 270 as shown in Figure 2) to the thermoelement couple.

Claim 50: The recitation "utilized as a resistive load for an electric component" has been construed as a process limitation that does not alter the overall physical structure of the claimed device and is, therefore, given little patentable weight. However, because the device of the Burward-Hoy combination is structurally the same as that instantly claimed, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the device of the Burward-Hoy combination would provide the claimed utility.

Claim 51: As to the recitation "voltage and current is generated...and is consumed by an external electric load", the rejection is as set forth above in claim 50

Claim 52: Burward-Hoy does not disclose that each dissimilar thermoelement is electrically bonded to each other at both the heat absorbing and heat rejecting junctions.

Buist discloses in Figure 2a that each dissimilar thermoelement (30, 32) is electrically bonded to each other (via metallizations 26, 28) at both the heat absorbing (cold core at metallization 28) and heat rejecting junctions (hot annular ring at metallization 26) (col. 2:56-col. 3: 44).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the apparatus of Burward-Hoy by incorporating the electrical bonding of Buist for reasons as set forth above in claim 43.

9. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burward-Hoy in combination with Buist as applied to claim 43 above, and further in view of Bhatia.

Burward-Hoy and Buist are as applied, argued and disclosed above, and incorporated herein.

Claim 49: The Burward-Hoy combination does not disclose that the electrically conductive member is electrically in series with an electrical load other than itself. Bhatia in Figure 2 discloses that the electrically conductive member (35) is electrically in series with an electrical load (circuit board 40) col. 3: 47-58).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the apparatus of the Burward-Hoy combination by incorporating the electrical load of Bhatia because Bhatia teaches that it would have been known to apply an electrically conductive member electrically in series with an electrical load to provide for operating the IC at significantly reduced temperatures thereby resulting in lower cost and more efficient heat dissipation, especially at the system level.

Allowable Subject Matter

10. Claims 1-4, 13-21 and 35-42 are allowable over the prior art of record.

11. Claims 6, 10, 11, 24, 26, 29, 44, 45, and 47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Indicating Allowable Subject Matter

12. The following is a statement of reasons for the indication of allowable subject matter:

U.S. Patent No. 3,635,037 issued to Hubert on 18 January 1972 discloses a doped region diffused onto and between a thermoelectric device and a heat exchanger creating a barrier layer wherein the barrier layer prevents electrical conductivity thereacross and functions as a metallic heat conductor and an almost perfect electrical insulator. In contrast, the instantly claimed invention requires a doped region diffused within the IC die's semiconductor substrate backside thereby creating a depletion layer between the substrate and the doped region.

Therefore, a search of the prior art of record failed to reveal or explicitly teach, alone or in combination, what is instantly claimed: in particular,

A heat dissipating IC device comprising at least one IC die comprising a semiconductor substrate including at least one circuitry layer with a hot region on at least one substrate face, a backside and a perimeter; a doped region diffused within the semiconductor substrate backside thereby creating a depletion layer between the substrate and doped region; and a voltage connected to the doped region, whereby the charge carrier flow, through the doped region of the substrate, travels in a direction from the hot region on the semiconductor substrate face outward toward the perimeter of the substrate face. For this reason, claim 1 and claims 2-4, which depend therefrom, are patentably distinct from the prior art of record.

U.S. patent Nos. 6,094, 919; 5,637,921; and 5,032,897 disclose thermocouple elements (n and p-type) electrically connected to conductors thereby creating a heat absorbing (cold side plate) junction and heat rejecting junction (hot side plate) and sandwiched between ceramic

(semiconductor) plates thereby creating a thermoelectric module; the thermoelectric module is coupled to the IC die's semiconductor substrate. In contrast, the instantly claimed invention requires bonding the conductors to the IC die's substrate to which are electrically connected the thermoelectric elements creating heat absorbing and heat rejecting junctions.

Therefore, a search of the prior art of record failed to reveal or explicitly teach, alone or in combination, what is instantly claimed: in particular,

A heat dissipating IC device comprising at least one IC die comprising a semiconductor substrate including at least one circuitry layer on at least one substrate face; at least one thermoelement couple, the couple comprised of the semiconductor substrate and at least one dissimilar conductor electrically bonded to the semiconductor substrate thereby creating junctions; and the thermoelement couple comprises at least one heat absorbing junction and at least one heat rejecting junction wherein the heat absorbing junction is positioned near the center of the substrate face and the heat rejecting junction is positioned neat the perimeter of the substrate. For this reason, claim 13 and claims 14-21, which depend therefrom, are patentably distinct from the prior art of record.

A method of manufacturing a heat dissipating IC device including at least one IC die comprising a semiconductor substrate including at least one circuitry layer on at least one substrate face, more than one thermoelement couple, each with at least one heat absorbing and one heat rejecting junction and p-type and n-type conductive dopants comprising selectively depositing the p and n-type dopants into at least one face of the substrate to form a pattern of p and n-type conductive thermoelements within the semiconductor substrate; and electrically bonding the p and n-type conductivity thermoelements at heat absorbing and heat rejecting

junctions to form thermoelements couples. For this reason, claim 35 and claims 36-42, which depend therefrom, are patentably distinct from the prior art of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas H Parsons whose telephone number is (703) 306-9072. The examiner can normally be reached on M-F (7:00-4:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Pat Ryan can be reached on (703) 308-2383. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9310 for regular communications and (703) 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0661.

Thomas H Parsons
Examiner
Art Unit 1745

March 5, 2003